REMARKS:

This paper is herewith filed in response to the Examiner's Office Action mailed on May 7, 2009 for the above-captioned U.S. Patent Application. This office action is a rejection of claims 1-2, 5-14, 17-24, 39-40, and 43-51of the application.

More specifically, the Examiner has rejected claims 1-2, 5-14, 17-24, 39-40, and 43-50 under 35 USC 103(a) as being unpatentable over Young (US6,346,832) in view of Chun (US6,294,933). The Applicants respectfully disagree with the rejection.

In addition, the Applicants note that the Examiner has indicated that claims 3-4, 15-16, and 41-42 are objected to as being dependent upon a rejected claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicants thank the Examiner for this indication of allowable subject matter.

Claims 1-24 and 39-54 have been amended for mere formality and to remove acronyms from the claims. Further, claims 39-52 and 54 have been amended to relate to an apparatus. These amendments are supported in at least paragraph [0009] of the published application. No new matter is added.

Regarding the rejection of claim 1 the Applicants note that claim 1 recites:

> A multi-mode input/output circuit, comprising at least one of transmitter circuitry or receiver circuitry, said transmitter circuitry configured to send data to another integrated circuit, and said receiver circuitry configured to receive data from another integrated circuit, said input/output circuit being constructed with complementary metal-oxide-semiconductor based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link.

In the rejection the Examiner states:

> "As per claims 1, 5-6, 13, 17, and 23, 39, and 43-44, Young disclosed a multi-mode Input/Output circuit for transmitting and receiving data between integrated circuits wherein each IC having at least one of

> transmitter circuitry (fig. 1/no. 10) or receiver circuitry (fig. 1/no. 12), the transmitter circuitry configured to send data to another IC and the receiver circuitry configured to receive data from another IC, and wherein the I/O circuit being construct with CMOS-based transistors that are selectively interconnected together by switches to operate as single-ended, current or voltage mode links, and as a single differential, current or voltage mode link (fig. 1, fig. 3, col. 2/ln. 8-43, col. 4/ln. 25-col. 5/ln. 17)," and
>
> "Young does not explicitly disclosed that the I/O circuit comprising switches to operate as two single-ended signaling. However, Chun taught such signaling (fig. 1, abstract, also see foreign search report). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention for Young to utilize such signaling method, as taught by Chun, in order provide a flexible interface signaling circuitry with reduce power consumption and cost."

The Applicants note that Young relates to a transmission circuit in which a high speed differential signal and a common mode signal are sent over the same two lines. Further, as cited Young discloses:

> "Transmission circuit 10 utilizes DATA 1, and DATA 2 to generate a pair of signals on WIRE 1 and WIRE 2 which contain both a differential signal and a common mode signal," (col. 2, lines 14-17); and
>
> "Thus, the transmission and receive circuits shown in FIG. 1 provide both a high speed differential signal and a common mode signal which is utilized as a single-ended input for single-ended amplifier 32," (col. 4, lines 9-12).

The Applicants note that here Young discloses that the common mode signal sent with the differential signal is utilized as an input for a single ended amplifier. Further, the Applicants submit that for at least the reason that, as stated above, the signals on WIRE 1 and WIRE 2 contain both a differential signal and a common mode signal, each of these signals are seen to contain a combined transmission.

Further, the Applicants submit that, for at least these reasons, Young is seen to merely disclose a single unidirectional operational mode, whereas, claim 1 relates to a multi-mode input/output circuit for transmitting and receiving data between integrated circuits.

Moreover, the Applicants note that Young discloses:

> In the case of an integrated circuit transmitting a differential signal, that means the integrated circuit itself has two output pins for each signal, and the pin count significantly impacts cost and reliability as well as size of the integrated circuit itself. The number of pins affects the cost of making the semiconductor wafers that have the integrated circuit die as well as the package which houses or carries the integrated circuit when shipped to the end user. The size aspect impacts the end user because the integrated circuit is generally located on a product. The available space on a printed circuit board that contains the integrated circuit in the product is typically desired to be as small as possible. It is advantageous if there is less space taken up by the integrated circuit," (emphasis added), (col. 1, lines 37-50).

Thus, it can be seen that, in Young, motivation for such a combined transmission appears to include a reduction in the number of pins and/or circuits, as well as a reduction in a size of the integrated circuits for the signaling.

The Applicants submit that, for at least this reason, one of ordinary skill in the art would not be motivated to add switches to the integrated circuits of Young in order to attempt to provide a multi-mode function, as appears to be argued in the rejection. This is seen to be the case for at least the reason that such an implementation would clearly go against the teachings of Young as it would likely at least increase the size of the integrated circuits.

With regards to where the rejection applies the signaling method of Chun to Young, the Applicants submit that even if Young and Chen were somehow combined, which is not agreed to as proper, the combination would still fail to disclose or suggest claim 1.

In the office action the Examiner admits that "Young does not explicitly disclosed that the I/O circuit comprising switches to operate as two single-ended signaling." The Applicants submit that Chun does not address this admitted shortfall of Young.

The Applicants note that, as cited, Chun discloses:

> "The switching action converts a single-ended input signal to a differential signal pair across the common resistive element. [and] A receiver converts the differential signal pair back to a single-ended output voltage signal," (emphasis added), (Abstract).

The Applicants submit that these operations of Chun, which relate to converting a single-ended input signal to a differential signal pair and back again, do not disclose or suggest at least where claim 1 recites in part:

> "said input/output circuit being constructed with complementary metal-oxide-semiconductor based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link"

The Applicants submit that Chun, as cited, is seen to merely disclose a switching action to convert a single-ended input signal to a differential signal pair and the differential signal pair back to a single-ended output voltage signal.

The Applicants do not find in Chun any disclosure or suggestion relating to selectively interconnecting transistors together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode links, as in claim 1.

The Applicants submit that Chun discloses a transmitter and receiver circuit. The transmitter circuit receives a single-ended signal and transmits the signal via differential signal traces. The receiver receives the differential signal traces and provides a related single ended output signal (see col. 3, lines 14-25). The Applicant submits that, here, Chun is operating in only one mode. Chun does not include any switching capabilities of the type claimed in the instant patent application, e.g., transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link.

Therefore, for at least the reasons stated above, the Applicants submit that the proposed combination of Young and Chun, though not agreed to as proper, would still fail to disclose or suggest claim 1. Thus, for at least this reason the rejection of claim 1 is seen to be improper and the rejection should be removed.

Further, the Applicants submit that for at least the reasons that independent claims 13 and 39 recite language similar to claim 1, as stated above, the references cited can not be seen to disclose or suggest these claims.

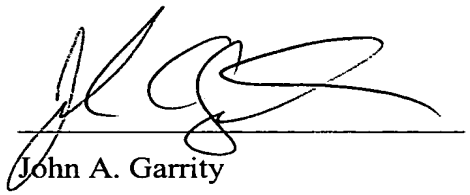
Further, the Applicants note that although not all the rejections in the Office Action are argued, the Applicants do not acquiesce to these rejections.

In addition, claims 2-12 and 52, claims 14-24 and 53, and claims 40-51 and 54 are seen to overcome the rejections for at least the reason that they depend from claims 1, 13, and 39, respectively.

Based on the above explanations and arguments, it is clear that the references cited cannot be seen to disclose or suggest claims 1-24 and 39-54. The Examiner is respectfully requested to reconsider and remove the rejections of claims 1-24 and 39-54 and to allow all of the pending claims 1-24 and 39-54 as now presented for examination.

For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record. Should any unresolved issue remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted:



7/21/2009

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450.

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